Claims

1. Carrier recovery means - in particular in a channel decoding unit and/or a digital demodulating unit being particularly provided in a digital broadcasting receiver - for recovering a carrier of a received digital input signal,

comprising at least first and second phase error detecting means (2, 4), in which

- said first or robust phase error detecting means (2) is adapted for detecting a first or robust estimate for the phase error of the received digital input signal and for generating and/or outputting a first or robust phase error signal being representative for said robust phase error,

- said second or frequency sensitive phase error detecting means (4) is adapted for receiving a phase error signal from said first phase error detecting means (2) and in particular said first or robust phase error signal and for deriving therefrom a second or frequency sensitive phase error signal which is representative at least for the sign of the frequency error or offset with respect to the received digital input signal and

- said second or frequency sensitive phase error signal is used to reduce the frequency error with respect to the received digital signal to enable locking to at least the carrier thereof.

2. Carrier recovery means according to claim 1, **characterized in** that

said second phase error detecting means (4) comprises at least a subtracting/differentiating unit (10), a first limiting unit (11), and an adding/integrating unit (12) which are in particular connected in series in that order.

3. Carrier recovery means according to claim 2, **characterized in** that

said subtracting/differentiating unit (10) is adapted to receive a phase error signal from said first phase error detecting means (2) and in particular said first or robust phase error signal as an input signal and to generate and/or output a difference/differential signal thereof.

4. Carrier recovery means according to claim 3, **characterized in** that

said first limiting unit (11) is adapted to receive said difference/differential signal as an input signal and to generate and/or output a limited signal thereof not exceeding given first lower and/or upper limits.

5. Carrier recovery means according to claim 4, **characterized in** that

said adding/integrating unit (12) is adapted to receive said limited difference/differential signal as an input signal and/or to generate and output a sum/integral signal thereof.

6. Carrier recovery means according to claim 5, **characterized in** that

a second limiting unit (13) is provided which is in particular connected in series to said adding/integrating unit (12) and

said second limiting unit (13) is adapted to receive said sum/integral signal as an input signal and to generate and/or output a limited signal thereof not exceeding given second lower and/or upper limits.

7. Carrier recovery means according to ~~any of the preceding~~ claims, **characterized in** that

said first or robust phase error detecting means (2) is adapted to generate and/or output a valid robust phase error signal of the received digital input signal when an amplitude of the received digital input signal is above a given threshold and

said second or frequency sensitive phase error detecting means (4) is adapted to use only said valid robust phase error signal as an input signal only for generating said second or frequency sensitive phase error signal.

8. Carrier recovery means according to ~~any of the preceding~~ claims, **characterized in** that

lock detector means (5) is provided which is adapted to receive a phase error signal and to generate and/or output a locking signal therefrom when said phase error signal and/or an average value thereof is beyond a given threshold.

9. Carrier recovery means according to claim 8, **characterized in** that

said locking detector means (5) is adapted to use said robust phase error signal and/or in particular said valid robust phase error signal supplied by said first or robust phase error detecting means (2).

10. Carrier recovery means according to claim 8 ~~or 9~~, **characterized in** that

third or precise phase error detecting means (3) is provided which is

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adapted for receiving said digital input signal and for generating and/or outputting a third or precise phase error signal thereof when said locking signal is generated and

said third or precise phase error signal is used to reduce at least the phase error of the received digital input signal to enable phase locking with the carrier.

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